

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE



Inventor: James D. Pylant et al.

Group Art Unit: 3721

Serial No.: 10/621,031

Examiner: Louis K. Huynh

Filing Date: July 14, 2003

Attorney Docket: PI-018

Title: **WAFER SHIPPER WITH ORIENTATION CONTROL**

**TRANSMITTAL**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

Attached is an Appeal Brief for the above-identified application. The Appeal Brief is being filed within the three month response period. In addition, no new claims are being added.

The authorization to charge the Notice of Appeal fee is provided on the Notice of Appeal that is being submitted herewith.

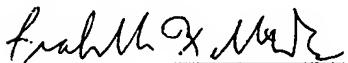
Respectfully submitted,



Isabelle R. McAndrews  
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Isabelle R. McAndrews

07-13-05

Date

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APPEAL BRIEF

Sir:

This Appeal Brief, which is being filed in triplicate, is accompanied by a Notice of Appeal, for the above-identified application.

I. Real Party in Interest

The Real Party in Interest in this Appeal is Peak Plastics and Metal Products (International) Limited, the assignee of the above-identified patent application.

II. Related Appeals and Interferences

No other appeal or interferences are known to Appellant which will directly affect, be directly affected by, or have a bearing on the Board's decision in this appeal.

### III. Status of Claims

The application includes claims 15 – 22. Claims 1 – 14 were cancelled and are not involved in this appeal.

Claims 15 -22 were finally rejected in the office action dated May 26, 2005 and are at issue in this Appeal. Claims 15 – 22 as now pending in the application are set forth below in the Appendix.

### IV. Status of Amendments

Entry of an amendment after the final office action dated May 26, 2005 was requested in an Amendment filed June 9, 2005, and was granted upon filing of the appeal (Advisory Action dated June 23, 2005). Claims 15, 19, and 22 in the Appendix include the amendment entered after the final rejection.

### V. Summary of the Invention

The invention is directed to a wafer container that stores wafers or wafer frames in a known orientation. (*Specification at page 5, last five lines of paragraph 20; i.e. lines 11 – 15 of page 5.*) At least one alignment artifact is present on each wafer or wafer frame (hereinafter wafer element). An alignment artifact is used for determining the position orientation of the wafer element in the container of the invention. (*Specification at page 3, lines 10 - 12.*)

The wafer containers have an orientation artifact that engages to one or more alignment artifacts on each wafer element. (*Specification at page 3, lines*

7 - 10.) Together, the orientation artifact and the alignment artifact ensure that all of the wafer elements are oriented in the same known orientation within the storage container. (*Specification at page 5, lines 11 - 15.*)

The invention is also directed to a wafer container that conforms to the outer dimension of the wafers. (*Specification at page 5, lines 9 - 11.*) The wafers are placed inside the container so that their alignment artifacts mate with at least one of the orientation artifacts on the container as shown in Fig. 4A. (*Specification at page 5, lines 19 – 22.*) Fig. 5 of the present application illustrates a top-view of Fig. 4A. In particular, alignment artifacts 68 and 70 are shown mated to orientation artifacts 54 and 56 respectively. (*Specification at page 5, paragraph 23, i.e. page 5, last four lines.*)

## VI. Issue on Appeal

Whether claims 15 – 22 are patentable under 35 USC 103(a) over Kawada (6,119,865) in view of Takeuchi et al. (5,238,876).

## VII. Grouping of the Claims

Claims 15 -18 stand or fall together and are referred to herein as Group I claims. Claims 19 -22, Group II claims, stand or fall together, but are separately patentable from Group I.

## VIII. Arguments

### A. Basis for Rejection is Improper

The Examiner's basis for rejecting the pending claims hinges on two assertions: 1) that the orientation of the wafer assemblies must be

known at all times during processing and/or storage; and 2) that the wafer assemblies of Takeuchi should have the same orientation when being placed into the container of Kawada. However, neither Takeuchi nor Kawada suggest either assertion. Moreover, there is no motivation to combine Takeuchi with Kawada to obtain the presently claimed invention. Assuming arguendo, that the skilled artisan would combine the teachings of Takeuchi with Kawada, the claimed invention would still not be obtained as explained below.

B. Claims 15 -18 are Patentable over Kawada in view of Takeuchi

Claims 15 -18 stand rejected under 35 USC 103(a) over Kawada in view of Takeuchi. This rejection should be reversed.

Kawada discloses a storage container for wafers that consists of slots or shelves on which each wafer is supported. It is not possible for these slots (16) to constitute orientation artifacts as suggested by the Examiner (*Office Action dated 01/14/2005 at page 2*) for at least two reasons (note paragraph 20 of the specification at page 5). First, slots (16) in Kawada's containers lack the type of contour that would permit engagement with a wafer element as recited in claim 15 of the present invention. Second, Kawada's slots do not function to prevent rotational movement of the wafers stored therein. The result is that Kawada's container stores wafers in dissimilar and unknown orientations.

The goal in Kawada is to separate each wafer from bonding to each other (col. Lines 22 – 25) due to shock or vibration. Kawada prevent such bonding by supporting each wafer on a pair of slots. However, in no case are the slots acting “to prevent substantial rotational movement” of each wafer within a storage chamber as recited in claim 15.

Nothing in Kawada suggests that partitioning slots 16 function as an orientation artifact. Slots 16 have the same flat contour throughout their length, and therefore do not provide “engagement of the at least one alignment artifact disposed on each wafer frame with at least one orientation artifact disposed within the storage container” as recited in all of the pending claims. Moreover, Kawada does not suggest that its container functions to orient each wafer in any particular orientation. In summary, Kawada simply lacks anything that would serve as an orientation artifact for mating with an alignment artifact on a wafer element, and that would prevent rotational movement of the stored wafers.

Takeuchi fails to remedy the deficiencies of Kawada. The Examiner has asserted that “the orientation of the wafer assemblies must be known at all times during processing and/or storage”. Takeuchi contradicts the Office Action because the orientation of each wafer assembly in Takeuchi is unknown, thereby necessitating a prealignment stage. In Takeuchi’s process, wafer frames are taken out of a container and then taken to a prealignment section where they are sequentially aligned in the direction  $\theta$ . (See U.S. Patent 5,238,876 at col. 5, lines 4-10.)

Conspicuously, Takeuchi does not disclose how his wafer frames would be oriented within a container. Nor does Takeuchi disclose the desirability of using notches 11a to discern orientation within a container. Claim 15 recites:

the step of sequentially placing including the step of engagement of the at least one alignment artifact disposed on each wafer frame with at least one orientation artifact disposed within the wafer storage container, thereby orienting each wafer frame in the wafer storage container

Takeuchi's notches (11a) do not ipso facto result in a known orientation. It is necessary in Takeuchi to remove his wafers out of their container and then orient the notched wafers. In addition, Kawada's container lacks any type of artifact that can engage with the notches of Takeuchi. Therefore, Appellants' invention is clearly not rendered obvious by Kawada in view of Takeuchi. Accordingly, Appellants submit that the rejection of claims 15 -18 under 35 USC 103(a) should be reversed.

#### C. Claims 19 -22 are Patentable over Kawada in view of Takeuchi

Claims 19 -22 stand rejected under 35 USC 103(a) over Kawada in view of Takeuchi. This rejection should also be reversed.

Claims 19 – 22 differ from Claims 15 -18 by reciting “a container that conforms to the outer dimension of the wafer elements”. Such a feature is absent from the applied prior art.

Kawada's container does not conform to the outer dimension of the wafer frames of Takeuchi. Claims 19 -22 also recite that “the alignment artifact of each wafer element mates with at least one

orientation artifact of the container.” In order for Kawada’s container to be “mate” with the notches 11a of Takeuchi, Kawada’s container must conform to the outer dimension of the wafer frames. This is clearly not the case as the wafer frames of Takeuchi would rest on slots 16, instead of mating with any one of the slots in Kawada.

The present invention is novel and non-obvious because the container of Kawada does not conform to the outer dimension of the wafer frames, and because Kawada lacks “at least one orientation artifact that is capable of engagement” with Takeuchi’s notches. Therefore, Appellants request the reversal of the 35 USC 103(a) rejection of claims 19 – 22 as well.

#### IX. Conclusion

For the foregoing reasons, it is submitted that the Examiner’s rejection of Claims 15- 22 is erroneous. Therefore reversal of the 35 USC 103(a) rejection is respectfully requested.

Respectfully submitted,



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## APPENDIX

15. A method of storing a plurality of wafers in a stack within a wafer storage container, the method comprising the steps of:

placing each wafer of said plurality of wafers on a corresponding wafer frame to obtain a plurality of wafer assemblies, each wafer frame including at least one alignment artifact disposed thereon, the step of placing resulting in adhesion between each wafer and corresponding wafer frame sufficient to prevent substantial movement of the wafer relative to the corresponding wafer frame;

sequentially placing each wafer assembly into a wafer storage chamber to form a stack wherein each wafer assembly has a known orientation that is visible when the chamber is uncovered, the step of sequentially placing including the step of engagement of the at least one alignment artifact disposed on each wafer frame with at least one orientation artifact disposed within the wafer storage container, thereby orienting each wafer frame in the wafer storage container and preventing substantial rotational movement of each wafer frame and the wafer disposed thereon within the storage chamber; and

covering the wafer storage chamber with a cover to fully enclose the stack.

16. The method of claim 15 wherein the step of placing comprises placing an adhesive film over an open area of each wafer frame.

17. The method of claim 15 wherein the step of placing further comprises the step of placing each wafer on the adhesive film.
18. The method of claim 15 wherein the step of sequentially placing each wafer assembly into the wafer storage chamber to form the stack comprises aligning a plurality of alignment artifacts disposed on each wafer frame with a corresponding plurality of orientation artifacts disposed within the wafer storage chamber.
19. A method of storing a stack of wafers in a wafer storage container, the method comprising the steps of:
  - providing a plurality of wafer elements, each wafer element having at least one alignment artifact on a wafer frame;
  - providing a container that conforms to the outer dimension of the wafer elements, wherein the container includes at least one orientation artifact that is capable of engagement with an alignment artifact of each wafer element;
  - placing the wafer elements in the container so that the alignment artifact of each wafer element mates with at least one orientation artifact of the container.
20. The method of storing a wafer stack in the wafer storage container of claim 19, wherein each wafer element has an orientation that is visible when the chamber is uncovered.

21. The method of storing a wafer stack in the wafer storage container of claim 19, wherein each wafer element has a known orientation that is visible when the chamber is uncovered.

22. The method of claim 19 wherein the step of placing the wafer elements into the wafer storage chamber comprises aligning a plurality of alignment artifacts with a corresponding plurality of orientation artifacts disposed within the wafer storage chamber.